REMARKS/ARGUMENTS

Claims 1-24 were pending in this application when last examined by the Examiner. Claims 1-20 and 22-24 have been amended. Claim 25 has been added. The amendments find full support in the original specification, claims, and drawings. No new matter has been added. In view of the above amendments and remarks that follow, reconsideration and an early indication of allowance of the now pending claims 1-25 are respectfully requested.

Claims 1-24 are objected to for numerous spelling and typographic errors. Applicant has now corrected the errors, and requests withdrawal of the objections of claims 1-24.

With respect to the Examiner's claim interpretation of the phrase "quasi microcomputer peripheral," Applicant has amended this claim language to "one or more devices." Applicant submits that although the now claimed "one or more devices" may encompass FPGAs, the claimed invention is not limited to FPGAs.

With respect to the Examiner's claim interpretation of the phrase "virtual input/output register," Applicant has amended this claim language to "virtual memory device." Applicant submits that although the now claimed "virtual memory device" may be implemented in an FPGA, it is not limited to only the FPGA, but may also be implemented in other devices disclosed in Applicant's specification.

Claim 9 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Applicant submits that this rejection is now obviated by the amendments made to independent claim 1 from which claim 9 depends. Accordingly, withdrawal of the rejection under 35 U.S.C. 112, second paragraph, is respectfully requested.

Claims 1 and 2 are rejected under 35 U.S.C. 102(b) as being anticipated by "RIFLE-62: A Flexible Environment for Prototyping Dynamically Reconfigurable Systems," by Vasilko et al. (Vasilko). Applicant respectfully traverses this rejection.

Claim 1, as amended, is directed to "[[a]] logic development system using an external microcomputer which replaces a built-in microcomputer incorporated in an existing electronic

control unit." The claimed "logic development system" includes "a mother board," "core board," "peripheral component interconnect (PCI) bus coupling said mother board and said core board," and an "interface board." The claimed "core board" includes "one or more devices which simulate, by software, peripheral devices of the built-in microcomputer so as to execute an input or output process, the core board further including a computing block and a second communication block." Claim 1 further recites that the "first communication block included in said mother board and each of said one or more devices included in said core board are coupled to each other over said PCI bus," and that the "communication block and each of said one or more devices transfer data to or from each other over said PCI bus." Support for these amendments if found in FIGS. 2 and 5, and in the specification on paragraphs 0076-0084.

Vasilko discloses an experimental board, referred to as the RIFLE-62 board, having dynamically reconfigurable FPGAs. Vasilko, however, fails to teach or suggest the use of the RIFLE-62 board in a microcomputer "which replaces a built-in microcomputer incorporated in an existing electronic control unit."

In addition, Vasilko describes that the RIFLE-62 board includes three types of FPGAs (XC6200, XC3000, and XC4013E), memory, address busses, dual clocks, and dedicated interfaces. The RIFLE-62 board, however, cannot be the claimed "core board" because it fails to include "one or more devices," "computing block," and "second communication block," as is now claimed in amended claim 1.

Furthermore, Vasilko fails to teach or suggest a "mother board" coupled to a "core board" over a "peripheral component interconnect (PCI) bus." Although Vasilko discloses a PCI interface, such interface is used to connect the board to a host computer system, and not to the claimed "mother board" where both the "mother board" and "core board" are included in a "microcomputer." Accordingly, claim 1 is now in condition for allowance.

Claim 2 includes the limitations of claim 1 which make claim 1 allowable. Accordingly, claim 2 is in condition for allowance for the reasons discussed above with respect to claim 1. In addition, claim 2 recites "a bus controller in said computing block interposed between said first communication block in said mother board and each of said one or more devices." The "first

communication block included in said mother board and said bus controller are coupled to each other over said PCI bus, and said bus controller and each of said one or more devices are coupled to each other over an internal bus." Furthermore, "said first communication bock and each of said one or more devices transfer data to or from each other by way of said PCI bus, bus controller, and internal bus." Support for these limitations are found in FIG. 6, and in the specification on paragraphs 0078-0080.

Vasilko fails to teach or suggest the additional limitations of claim 2. Vasilko discloses a 32-bit PCI interface and a microprocessor interface on the RIFLE-62 board. (See, section 3.5). However, the disclosed interfaces are used to directly write and read data to and from the FPGAs. Nothing in Vasilko teaches or suggests the claimed "bus controller" for controlling the data flow of data transmitted to and from the core board and mother board via the PCI bus. Accordingly, claim 2 is also in condition for allowance for these added limitations.

Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Vasilko. Claims 4-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Vasilko in view of U.S. Patent No. 6,356,823 (Iannotti). Claims 20 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Vasilko in view of U.S. Patent No. 5,908,455 (Parvahan).

Claims 3, 4-8, and 20-21 are in condition for allowance because they depend on an allowable base claim, and for the additional limitations that they contain.

Claims 9-19 and 22-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Vasilko in view of U.S. Patent No. 5,864,712 (Carmichael). Applicant respectfully traverses this rejection.

Independent claims 22 and 23 include the limitations of claim 1 which make claim 1 allowable. Accordingly, claims 22 and 23 are in condition for allowance.

Claims 9-19 and 24 are in condition for allowance because they depend on an allowable base claim, and for the additional limitations that they contain.

Claim 25 is new in this application. Claim 25 is in condition for allowance because it depends on an allowable base claim, and for the additional limitations that it contains. Specifically, claim 25 adds the limitation that "the computing block is a microcomputer, and the

bus controller in the microcomputer is configured to control flow of information between the mother board and the one or more devices."

In view of the above amendments and remarks, reconsideration and an early indication of allowance of the now-pending claims 1-25 are respectfully requested.

Respectfully submitted,

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